IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Applicants :	CHEN ET AL.	)	Confirmation No. 8561
		)	
Serial No. :	10/733,721	)	Examiner: Evan Pert
		)	Group Art Unit: 2826
Filed :	11 December 2003.	)	
		)	TKHR Ref. 250914-1010
For :	Method of Forming Poly-Silicone Thin Film Transistors	)	Tsai, Lee & Chen Ref. NP-1812-US
		)	
		)	

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Office Action February 10, 2006 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AMENDMENT

In The Claims:

The pending claims are listed as follows:

1. (Currently amended): A method of forming poly-silicon thin film transistors, comprising the steps of:

providing an amorphous silicon thin film transistor having a gate metal and a source/drain metal; and

heating the amorphous silicon thin film transistor with an IR energy source to change the amorphous silicon thin film transistor into a poly-silicon thin film transistor.

2. (Original): The method of claim 1, wherein the amorphous silicon thin film transistor comprises a bottom-gate or top-gate structural type.

3. (Original): The method of claim 2, wherein the bottom-gate structural type comprises a back channel etch (BCE) or a channel protect (CHP) structural type.

4. (Currently amended): The method of claim 3, wherein forming the back channel etch (BCE) structural type comprises steps of:

forming the [[a]] gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a doped amorphous silicon layer in turn on the gate metal and the substrate simultaneously;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming the source/drain metal on the doped amorphous silicon layer;

patterning the [[a]] source/drain metal to form a data line; and

patterning the doped amorphous silicon layer to define a channel region.

5. (Withdrawn): The method of claim 3, wherein forming the channel protect (CHP) structural type comprises steps of:

forming a gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a protective layer in turn on the gate metal and the substrate simultaneously;

patterning the protective layer to form an etching stop layer;

forming a doped amorphous silicon layer on the amorphous silicon layer and the etching stop layer;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming a source/drain metal on the doped amorphous silicon layer;

patterning the source/drain metal to form a data line; and

patterning the doped amorphous silicon layer to define a channel region.

6. (Withdrawn): The method of claim 2, wherein forming the top-gate structural type comprises steps of:

forming a buffer layer on a substrate;

forming an amorphous silicon layer on the buffer layer;

forming a gate insulator on the amorphous silicon layer;

forming a gate metal on the gate insulator;

utilizing the gate metal as a mask to ion implant the amorphous silicon layer on two sides of the gate metal for defining a source/drain region in the amorphous silicon layer;

forming a dielectric interlayer on the gate metal and the gate insulator;

patterning the dielectric interlayer to form contact holes;

forming a source/drain metal on the dielectric interlayer and in the contact holes to connect the source/drain region in the amorphous silicon layer; and

patterning the source/drain metal to form a data line.

7. (Currently amended): The method of claim 1, wherein the step of heating with the IR energy source comprises a pulsed rapid thermal processing (PRTP) technology.

8. (Currently amended): A method of forming poly-silicon thin film transistors employed for flat panel display, comprising the steps of:

forming a gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a doped amorphous silicon layer in turn on the gate metal and the substrate simultaneously;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming a source/drain metal on the doped amorphous silicon layer;

patterning the source/drain metal to form a data line;

patterning the doped amorphous silicon layer to define a channel region; and

performing a heating process with an IR energy source, wherein the gate metal and the source/drain metal rapidly absorb heat energy from the IR energy source and transfer the heat energy to the amorphous silicon layer, and the amorphous silicon layer subsequently crystallizes to become a poly-silicon layer.

9. (Original): The method of claim 8, wherein the gate metal is a metal material with good IR absorption and thermal stability.

10. (Original): The method of claim 9, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

11. (Original): The method of claim 8, wherein the source/drain metal is a metal material with good IR absorption and thermal stability.

12. (Original): The method of claim 11, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

13. (Currently amended): The method of claim 8, wherein the heating process with the IR energy source comprises a pulsed rapid thermal processing (PRTP) technology.

14-20. (Canceled)

REMARKS AND RESPONSES

The Examiner is thanked for the thorough examination of the present application, and the indication that claims 1-4 and 7-13 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112, second paragraph. Accordingly, claims 1 and 8 have been amended to address and overcome the rejections under 35 U.S.C. §112, second paragraph. Hence, the amended claims 1 and 8 are allowable, and dependent claims 2-4 and 7, which depend from claim 1, and claims 9-13, which depend from claim 8, overcome the rejection.

Claim Rejection - 35 U.S.C. §112, Second Paragraph

With respect to the Office Action, the Office Action rejected claims 1-5 and 7-13 under 35 U.S.C. §112 as being indefinite. Specially, the Office Action stated that claims 1 and 8 were potentially ambiguous since "IR" was not definitely recited. In response, Applicant amends claims 1 and 8 to define "an IR energy source" as recommended by the Examiner. In view of this amendment, it is respectfully submitted that claims 1 and 8 overcome the rejections under 35 U.S.C. § 112, second paragraph.

The Office Action also alleged that the feature of "providing an amorphous silicon thin film transistor" is ambiguous. In response, Applicant has amended this feature in claim 1 to define the claimed thin film transistor as "having a gate metal and a source/drain metal." As the Office Action indicated that the claimed structure was implied to provide a gate and source/drain metal, as amended, claim 1 overcomes the noted rejection.

As all relevant claims have been amended to overcome the rejections under 35 U.S.C. § 112, second paragraph, and no art-based rejections have been made, Applicant respectfully submits that all claims are now in condition for allowance.

Cited Art

The cited art made of record, but not relied upon, has been considered but is not believed to impact the patentability of the pending claims.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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